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## CMOS PIN Phototransistors for High-Speed Photosensitive Applications

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### Abstract

This work reports on two  $40 \times 40 \mu\text{m}^2$  high-speed pnp phototransistors built in a standard  $0.18 \mu\text{m}$  CMOS process without modifications. The phototransistors were implanted on wafer consisting of a  $\text{p}^+$  bulk with a  $\text{p}^-$  epitaxial layer on top of it. Bandwidths up to 50 MHz and a gain in responsivity of more than a factor of 3 at 850 nm light compared to the photodetector presented in [1] are achieved. Due to the achieved measurements, these phototransistors are well suited for high speed photosensitive applications where inherent amplification is needed like light barriers, image sensors, high speed opto-couplers, etc.

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**Keywords:** CMOS; BJT; Phototransistors; PNP; PIN; NIR; OEIC; Silicon

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### 1. Introduction

The conversion of optical into electrical signals has become a major trend in the last decades. This conversion can be done by means of pn photodiodes, pin photodiodes, avalanche photodiodes (APDs), phototransistors (PT), etc. Pn and pin photodiodes are the most common photodetectors implemented in CMOS. However, due to their structure, they cannot exceed the maximum responsivity (e.g. 0.65 A/W for 850 nm light) for quantum efficiency  $\eta=1$ . A pn photodiode with a responsivity of 0.5 A/W and a bandwidth of 1.6 MHz at 780 nm is reported in [1]. APDs and PT avoid this limitation by their inherent gain mechanisms. The most important advantage of PT over APDs for red and near-infrared light is that they do not need such high voltages like APDs for the amplification. A conventional pnp PT consists of a photodiode, built by the base-collector region and an

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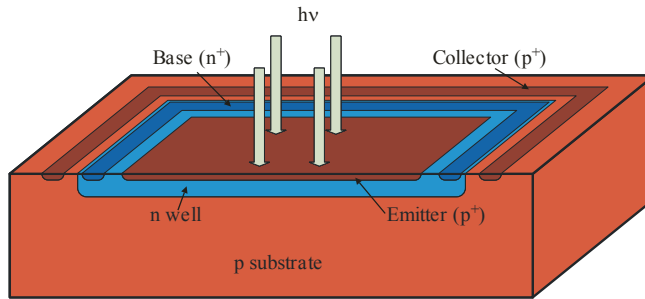


Fig. 1. Cross section of a conventional pnp phototransistor integrated in CMOS

internal bipolar transistor for the amplification (Fig. 1). Reference [2] reports on a pnp PT using buried  $n^+$  collector stripes of a SiGe npn transistor in  $0.35\ \mu\text{m}$  BiCMOS as a base achieving a bandwidth of 4.2 MHz at 850 nm. In [3] and [4]  $0.6\ \mu\text{m}$  CMOS pnp PIN PTs with a special wafer and bandwidths up to 14 MHz were presented.

## 2. Device Characteristics

Here we introduce  $40 \times 40\ \mu\text{m}^2$  speed optimized pnp PTs in a  $0.18\ \mu\text{m}$  CMOS process without process modifications. An OPTO ASIC wafer with a  $15\ \mu\text{m}$  thick  $p^-$  epitaxial layer with a doping concentration below  $5 \times 10^{13}\ \text{cm}^{-3}$  on top of the  $p^+$  bulk was used for implementation. This additional epitaxial layer leads to a thicker space-charge region in the base collector junction and thus to a smaller junction capacitance. The -3 dB bandwidth of the phototransistors depends strongly on the base-emitter and base-collector junction capacitances:

$$f_{-3\text{dB}} \sim \frac{1}{C_{BE} + C_{BC}} \quad (1)$$

For speed optimization the PTs were built with small emitter and small base areas to reduce the capacitances. Thereby, the emitter was implanted by a  $p^+$  layer and the base by a small n-well under the emitter. The small layout of the base and the emitter leads to an increased bandwidth but also to a small responsivity. The two presented phototransistors (PT<sub>EDGE</sub> and PT<sub>QUAD</sub>) have a  $p^+$  emitter at the edge and one emitter in each quadrant of the photosensitive area, respectively (Fig. 2).

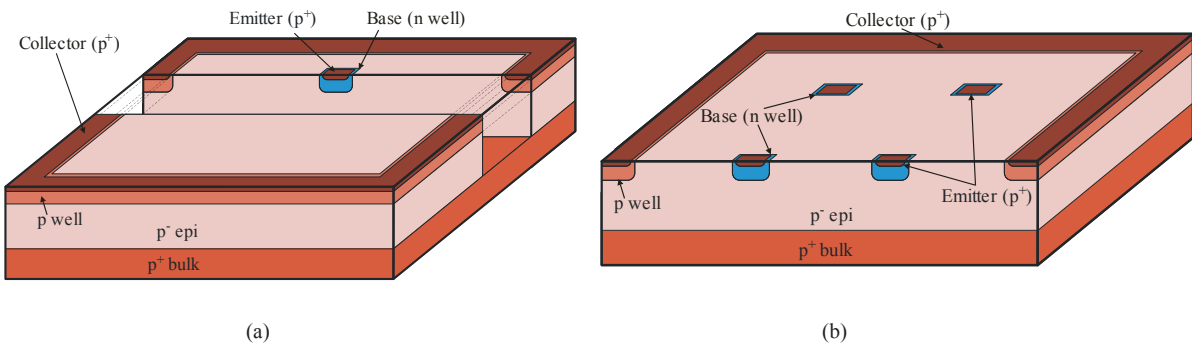


Fig. 2. 3D depiction of both presented phototransistors: (a) PT<sub>EDGE</sub> (b) PT<sub>QUAD</sub>

### 3. Measured Results

Optical responsivity, bandwidth and rise time measurements were done to characterize both PTs. Thereby an 850 nm laser with an extinction ratio of 1.48 and an optical power of -15.8 dBm was used.

#### 3.1. Responsivity measurements

The responsivity measurements were done at three different collector-emitter voltages  $V_{CE}$  (-2 V, -5 V and -10 V) and floating base. Due to the small base an inhomogeneous electric field is formed in the base-collector junction area which is the reason for a not fully depleted  $p^-$  epi layer. This fact leads furthermore to a higher recombination probability of the photogenerated charges in the non-depleted area of the collector and thus to a reduced responsivity. The PT<sub>QUAD</sub> device has more emitter/base area and thus a larger responsivity. Maximal responsivities up to 1.78 A/W and 1.28 A/W were achieved for the PT<sub>QUAD</sub> and PT<sub>EDGE</sub> device, respectively. Responsivity values for other  $V_{CE}$  voltages are shown in Tab. 1.

#### 3.2. Bandwidth and rise time measurements

An advantage of the small emitter and base area are smaller junction capacitances and thus according to equation (1) a higher -3 dB bandwidth. The bandwidths were measured similar to the responsivity measurements at three different  $V_{CE}$  voltages. At higher  $V_{CE}$  voltages the PTs show higher bandwidths since the higher voltage leads to thicker space-charge regions and thus to smaller junction capacitances. Bandwidths up to 50 MHz at  $V_{CE} = -10$  V were achieved for the PT<sub>EDGE</sub> device (Tab. 2). Fig. 3a depicts the frequency response of this device. PT<sub>QUAD</sub> shows for small voltages higher bandwidths due to shorter diffusion lengths of the photogenerated charges. Corresponding rise times down to 15 ns were measured and are shown in Tab. 3. For the bandwidth measurements a setup with a vector network analyser was used. The measurement setup is depicted in Fig. 3b.

Table 1. Responsivities for both presented phototransistors for different  $V_{CE}$  voltages at 850 nm light and -15.8 dBm optical power

Structure	$V_{CE} = -2V$	$V_{CE} = -5V$	$V_{CE} = -10V$
PT <sub>EDGE</sub>	1.11 A/W	1.19 A/W	1.28 A/W
PT <sub>QUAD</sub>	1.70 A/W	1.74 A/W	1.78 A/W

Table 2. Bandwidths for both presented phototransistors for different  $V_{CE}$  voltages at 850 nm light

Structure	$V_{CE} = -2V$	$V_{CE} = -5V$	$V_{CE} = -10V$
PT <sub>EDGE</sub>	12.0 MHz	25.1 MHz	50.0 MHz
PT <sub>QUAD</sub>	19.1 MHz	25.7 MHz	37.2 MHz

Table 3. Rise times for both presented phototransistors for different  $V_{CE}$  voltages at 850 nm light and -15.8 dBm optical power

Structure	$V_{CE} = -2V$	$V_{CE} = -5V$	$V_{CE} = -10V$
PT <sub>EDGE</sub>	33 ns	17 ns	15 ns
PT <sub>QUAD</sub>	24 ns	18 ns	16 ns

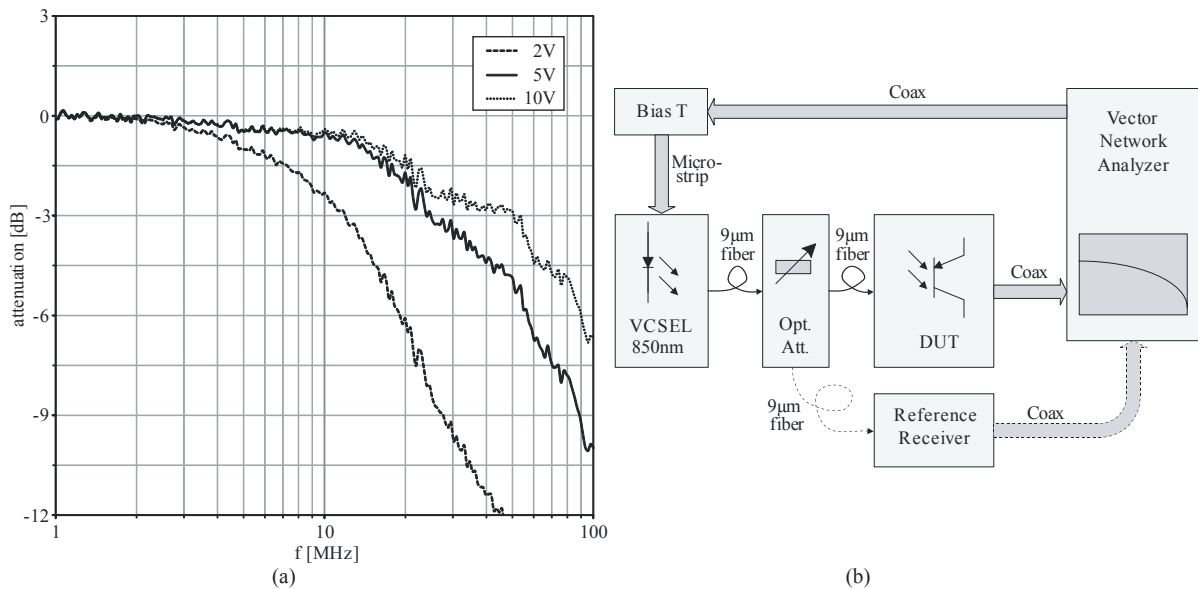


Fig. 3. (a) Frequency response of the PT<sub>EDGE</sub> phototransistor at three different  $V_{CE}$  (b) Setup for frequency response measurements

#### 4. Conclusion

We present two speed optimized pnp bipolar type phototransistors built in a  $0.18\ \mu\text{m}$  CMOS process without process modification. To achieve high bandwidths the phototransistors were implanted in a low doped p epitaxial layer on top of a  $p^+$  substrate wafer. A maximal responsivity of  $1.78\ \text{A/W}$  was achieved. However, this value is more than three times larger compared with standard pn diodes like that presented in [1]. Bandwidths up to 50 MHz were achieved due to small base-emitter and base-collector capacitances caused by the low doped p epitaxial layer and the small emitter sizes of each device. The presented phototransistors are convenient for applications where photocurrent amplification is beneficial and a higher bandwidth compared to pn diodes is needed.

#### Acknowledgements

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